CLAIMS

What is claimed is:

1. An amplifier circuit comprising:

two operational amplifiers, each operational amplifier comprising:

a transconductance stage, having an inverting input, a non-inverting input, and having an output forming a gain node; and

a buffer connecting the gain node to an output of the operational amplifier;

an inverter having an input connected to the gain node, and having an output;

a first compensation capacitor connecting the output of the inverter of a first of the two operational amplifiers to the input of the inverter of a second of the two operational amplifiers; and

a second compensation capacitor connecting the output of the inverter of the second of the two operational amplifiers to the input of the inverter of the first of the two operational amplifiers.

2. The amplifier circuit of claim 1, further comprising:

a third compensation capacitor connecting the gain node of the first of the two operational amplifiers to a first power supply potential; and

a fourth compensation capacitor connecting the gain node of the second of the two operational amplifiers to the first power supply potential.

3. The amplifier circuit of claim 1, further comprising:

a third compensation capacitor connecting the gain node of the first of the two operational amplifiers to the gain node of the second of the two operational amplifiers.

4. An amplifier circuit comprising:

two current feedback amplifiers, each current feedback amplifier comprising:

a first transistor (501,551) having a base forming a non-inverting input (IN_A+,IN_B+), a collector connected to a first power supply potential (Vcc), and having an emitter;

a first current sink (506,556) connecting the emitter of the first transistor to a second power supply potential (Vee);

a second transistor (502,552) having a base connected to the based of the first transistor (501,551), a collector connected to the second power supply potential (Vee), and having an emitter;

a second current sink (508,558) connecting the emitter of the second transistor (502,552) to the first power supply potential (Vcc);

a third transistor (503,553) having a base connected to the emitter of the second transistor (502,552), an emitter forming an inverting input (IN_A-,IN_B-), and a collector;

a fourth transistor (504,554) having a base connected to the emitter of the first transistor (501,551), an emitter connected to the emitter of the third transistor (503,553), and having a collector;

a first current mirror (510,560) having an input terminal connected to the collector of the third transistor (503,553), and having an output terminal;

a second current mirror (512,562) having an input terminal connected to the collector of the fourth transistor (504,554), and having an output terminal connected to the output terminal of the first current mirror (510,560) forming a gain node (n405,n415); and

a buffer (409,419) having an input connected to the gain node (n405,n415) and an output forming an output (OUT_A,OUT_B) of the current feedback amplifier;

a first common mode compensation capacitor (514) having a first terminal connected to the input terminal of the first current mirror (510) of a first one of the two current feedback amplifiers (AMP_A 400), and a second terminal connected to the gain node (n415) of a second one of the two current feedback amplifiers (AMP_B 460);

a second common mode compensation capacitor (516) having a first terminal connected

to the input terminal of the second current mirror (512) of the first one of the two current feedback amplifiers (AMP_A 400), and a second terminal connected to the gain node (n415) of the second one of the two current feedback amplifiers (AMP_B 460);

a third common mode compensation capacitor (564) having a first terminal connected to the input terminal of the first current mirror (560) of the second one of the two current feedback amplifiers (AMP_B 460), and a second terminal connected to the gain node (n405) of the first one of the two current feedback amplifiers (AMP_A 400); and

a fourth common mode compensation capacitor (566) having a first terminal connected to the input terminal of the second current mirror (562) of the second one of the two current feedback amplifiers (AMP_B 460), and a second terminal connected to the gain node (n405) of the first one of the two current feedback amplifiers (AMP_A 400).

5. The amplifier circuit of claim 4, further comprising:

a first differential mode compensation capacitor (402) connecting the gain node of the first of the two current feedback amplifiers (AMP_A 400) to the second power supply potential (Vee); and

a second differential mode compensation capacitor (412) connecting the gain node of the second of the two current feedback amplifiers (AMP_B 460) to the second power supply potential (Vee).

6. The amplifier circuit of claim 4, further comprising:

a first differential mode compensation capacitor (601) connecting the gain node to the input terminal of the first current mirror (510) of the first of the two current feedback amplifiers (AMP_A 400);

a second differential mode compensation capacitor (602) connecting the gain node to the input terminal of the second current mirror (512) of the first of the two current feedback amplifiers (AMP_A 400);

a third differential mode compensation capacitor (604) connecting the gain node to the input terminal of the first current mirror (560) of the second of the two current feedback amplifiers (AMP_B 460); and

a fourth differential mode compensation capacitor (606) connecting the gain node to the input terminal of the second current mirror (562) of the second of the two current feedback amplifiers (AMP_B 460).

7. The amplifier circuit of claim 4, further comprising:

a differential mode compensation capacitor (709) connecting the gain node of the first of the two current feedback amplifiers (AMP_A 400) to the gain node of the second of the two current feedback amplifiers (AMP_B 460).

8. An amplifier circuit comprising:

two differential amplifiers, each differential amplifier comprising:

a first transistor (801,821) having a gate forming a non-inverting input (IN_A+,IN_B+), and having a source and a drain;

a second transistor (802, 822) having a gate forming an inverting input (IN_A-,IN_B-), and having a source connected to the source of the first transistor (801,821), and having a drain forming an inverting output gain node (n405, n415);

a current sink (806,826) connecting the source of the first and second transistors to a first power supply potential (V_{SS});

a current mirror (804,824) having an input terminal connected to the drain of the first transistor (801,821), and an output terminal connected to the gain node (n405,n415);

a buffer (409,419) having an input connected to the gain node (n405,n415) and an output forming an output (OUT_A,OUT_B) of the differential amplifier;

a first common mode compensation capacitor (408) having a first terminal connected to the input terminal of the current mirror (804) of a first one of the two differential amplifiers

(AMP_A 400), and a second terminal connected to the gain node (n415) of a second one of the two differential amplifiers (AMP_B 460); and

a second common mode compensation capacitor (418) having a first terminal connected to the input terminal of the current mirror (824) of the second one of the two differential amplifiers (AMP_B 460), and a second terminal connected to the gain node (n405) of the first one of the two current feedback amplifiers (AMP_A 400).

9. The amplifier circuit of claim 8, further comprising:

a first differential mode compensation capacitor (402) connecting the gain node of the first of the two differential amplifiers (AMP_A 400) to the first power supply potential (Vss); and

a second differential mode compensation capacitor (412) connecting the gain node of the second of the two differential amplifiers (AMP_B 460) to the first power supply potential (Vss).

10. The amplifier circuit of claim 8, further comprising:

a first differential mode compensation capacitor (1002) connecting the gain node (n405) to the drain of the first transistor (801) in the first of the two differential amplifiers (AMP_A 400); and

a second differential mode compensation capacitor (1004) connecting the gain node (n415) to the drain of the first transistor (821) in the second of the two differential amplifiers (AMP_B 460).

11. The amplifier circuit of claim 8, further comprising:

a differential mode compensation capacitor (709) connecting the gain node of the first of the two differential amplifiers (AMP_A 400) to the gain node of the second of the two differential amplifiers (AMP_B 460).